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10/002,461	11/01/2001	Keith R. Slavin	DB000955-000	5286

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EXAMINER	
ELMORE, REBA I	

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 09/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/002,461	SLAVIN, KEITH R.	
	Examiner	Art Unit	
	Reba I. Elmore	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *March 12, 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/31/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-44 are presented for examination.

Drawings

2. Figure 6 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

5. Claims 1-29, 31-34, 36-42 and 44 are rejected under 35 U.S.C. 102(e) as being anticipated by Hariguchi et al. (P/N 6,665,297)

6. Hariguchi teaches the invention (claim 1) as claimed including a method for using a CAM for routing IP addresses, the method comprising:

inputting an input word to a plurality of hash circuits, each hash circuit being responsive to a different portion of the input word (e.g., see Figure 7, element 204);

outputting a hash signal from each hash circuit (e.g., see Figure 7, element 204);

enabling portions of a CAM in response to the hash signals (e.g., see Figures 3-4 and 7);

inputting the input word to the CAM (e.g., see Figure 3);

comparing the input word in the enabled portions of the CAM (e.g., see Figure 4); and,

outputting information responsive to the comparing step (e.g., see Figure 4).

As to claim 2, Hariguchi teaches assigning a mask to each hash circuit such that each hash circuit is responsive to a different n-bit portion of the input word (e.g., see Figure 4).

As to claim 3, Hariguchi teaches inputting the least significant n bits of the input word to a memory and wherein the outputting step includes selecting between information responsive to a match being found in the memory and information responsive to a match being found in the CAM (e.g., see Figures 2A-2B).

As to claim 4, Hariguchi teaches delaying the inputting of the input work to the CAM until the enabling step is completed (e.g., see col. 4, line 31 to col. 5, line 63).

As to claim 5, Hariguchi teaches enabling includes using the hash signals to select from a plurality of stored signals, and using the selected stored signals to enable a portion of the CAM (e.g., see col. 4, line 31 to col. 5, line 63).

As to claim 6, Hariguchi teaches using the selected stored signals includes using a starting index and a run length (e.g., see col. 6, lines 25-39).

As to claim 7, Hariguchi teaches using the selected stored signals includes using a starting index and an ending index (e.g., see Figure 5).

7. Hariguchi teaches the invention (claim 8) as claimed including a method of operation a CAM comprising:

hashing a comparand word (e.g., see Figures 4-5);

precharging certain portions of a CAM in response to the hashing step (e.g., see Figure 7, element 206); and,

inputting the comparand word to the CAM (e.g., see Figures 4-5).

As to claim 9, Hariguchi teaches the hashing step includes the steps of hashing different n-bit portions of the comparand word (e.g., see Figure 4).

As to claim 10, Hariguchi teaches the steps of inputting the least significant n bits of the comparand word to a memory and outputting information responsive to either a match being found in the memory and a match being found in the CAM (e.g., see Figures 2A-2B).

As to claim 11, Hariguchi teaches the step of delaying the inputting of the comparand word to the CAM until the precharging step is completed (e.g., see col. 4, line 31 to col. 5, line 63).

As to claim 12, Hariguchi teaches the precharging step includes using the hash signals to select from a plurality of stored signals and using the selected stored signals to precharge portions of the CAM (e.g., see col. 4, line 31 to col. 5, line 63).

As to claim 13, Hariguchi teaches using the selected stored signals includes using a starting index and a run length (e.g., see col. 6, lines 25-39).

As to claim 14, Hariguchi teaches using the selected stored signals includes using a starting index and an ending index (e.g., see Figure 5).

8. Hariguchi teaches the invention (claim 15) as claimed including a method of operating a CAM for processing address information comprising:

inputting an Internet address to a plurality of hash circuits, each hash circuit being responsive to a different portion of the address (e.g., see Figures 2A-2B);

outputting a hash signal from each hash circuit (e.g., see Figures 2A-2B);

using the hash signals to identify portions of a CAM (e.g., see Figures 2A-2B);

inputting the address to the CAM (e.g., see Figures 2A-2B);

comparing the address in only the identified portions of the CAM (e.g., see Figures 2A-2B); and,

outputting port information in response to a match being found in the CAM (e.g., see Figures 2A-2B).

As to claim 16, Hariguchi teaches assigning a mask to each hash circuit such that each hash circuit is responsive to a different n-bit portion of the address (e.g., see Figure 4).

As to claim 17, Hariguchi teaches the step of inputting the least significant n bits of the address to a memory and wherein the outputting step includes the step of selecting between port information associated with a match in the memory and port information associated with a match in the CAM (e.g., see Figures 2A-2B).

As to claim 18, Hariguchi teaches delaying the inputting of the address of the CAM until portions of the CAM have been precharged in responsive to the hash signals (e.g., see col. 4, line 31 to col. 5, line 63).

As to claim 19, Hariguchi teaches using the hash signals includes the steps of using the hash signals to select from a plurality of stored signals and using the selected stored signals to precharge portions of the CAM (e.g., see col. 4, line 31 to col. 5, line 63).

As to claim 20, Hariguchi teaches using the selected stored signals includes using a starting index and a run length (e.g., see col. 6, lines 25-39).

As to claim 21, Hariguchi teaches using the selected stored signals includes using a starting index and an ending index (e.g., see Figure 5).

9. Hariguchi teaches the invention (claim 22) as claimed including a method of operating a CAM for processing address information comprising:

hashing different prefixes within an Internet address (e.g., see Figures 2A-2B);

precharging certain portions of a CAM in response to the hashing step (e.g., see Figures 3-4 and 7);

comparing the Internet address in the precharged portions of the CAM (e.g., see Figure 4); and,

outputting information in response to a match being found in the CAM (e.g., see Figure 4).

As to claim 23, Hariguchi teaches the step of inputting the least significant n bits of the address to a memory and wherein the step of outputting information includes the step of selecting between information associated with a match in the memory and information associated with a match in the CAM (e.g., see Figures 2A-2B).

As to claim 24, Hariguchi teaches delaying the comparing step until the precharging step is completed (e.g., see col. 4, line 31 to col. 5, line 63).

As to claim 25, Hariguchi teaches the precharging step includes using the hash signals to select from a plurality of stored signals and using the selected stored signals to precharge portions of the CAM (e.g., see col. 4, line 31 to col. 5, line 63).

As to claim 26, Hariguchi teaches using the selected stored signals includes using a starting index and a run length (e.g., see col. 6, lines 25-39).

As to claim 27, Hariguchi teaches using the selected stored signals includes using a starting index and an ending index (e.g., see Figure 5).

10. Hariguchi teaches the invention (claim 28) as claimed including a circuit comprising:

a CAM for receiving a comparand word (e.g., see Figures 4-5);

a plurality of hash circuits connected in parallel, each for producing a hash signal in response to a portion of the comparand word (e.g., see Figures 2A-2B and 7); and,

a circuit, responsive to the hash signals, for precharging portions of the CAM (e.g., see col. 4, line 31 to col. 5, line 63).

As to claim 29, Hariguchi teaches the circuit responsive to the hash signals includes a plurality of memory devices responsive to the hash signals and enable logic responsive to the plurality of memories (e.g., see Figures 2A-2B and 3-4).

As to claim 31, Hariguchi teaches an output memory device responsive to the CAM for outputting information in response to a match in the CAM (e.g., see col. 4, line 31 to col. 5, line 63).

As to claim 32, Hariguchi teaches an input memory device responsive to a portion of the comparand work and a switch responsive to the input memory device and the output memory device (e.g., see col. 4, line 31 to col. 5, line 63).

As to claim 33, Hariguchi teaches the circuit further comprises a processor, the CAM, the plurality of hash circuits with the circuit being responsive to the hash circuits receiving information from the processor (e.g., see Figures 2A-2B).

11. Hariguchi teaches the invention (claim 34) as claimed including a circuit comprising:

a CAM (e.g., see Figures 2A-2B);

a plurality of hash circuits each for producing a hash signal in response to a portion of a comparand word (e.g., see Figures 2A-2B).

a plurality of memory devices responsive to the hash circuits (e.g., see Figures 2A-2B).

enable logic, responsive to the plurality of memory devices, for enabling portions of the CAM (e.g., see Figures 2A-2B); and,

a delay circuit for inputting the comparand word to the CAM (e.g., see Figures 2A-2B).

As to claim 36, Hariguchi teaches an output memory device responsive to the CAM for outputting information in response to a match in the CAM (e.g., see Figures 2A-2B).

As to claim 37, Hariguchi teaches an input memory device responsive to a portion of the comparand word and a switch responsive to the input memory device and the output memory device (e.g., see Figures 2A-2B).

As to claim 38, Hariguchi teaches a processor for initializing the hash circuits, the plurality of memory devices and the CAM (e.g., see Figures 2A-2B).

12. Hariguchi teaches the invention (claim 39) as claimed including a method comprising:

receiving routing information (e.g., see Figures 2A-2B).

mapping destinations to ports (e.g., see Figure 3);

hashing network addresses (e.g., see Figures 4-5);

loading hash values and address prefixes into a hash table (e.g., see Figures 4-5);

linking routing addresses and port information to the hash values (e.g., see Figures 4-5); and,

loading information from the hash table into a CAM (e.g., see Figures 4-5).

As to claim 40, Hariguchi teaches confirming that all network addresses for each prefix are unique (e.g., see col. 5, line 7 to col. 6, line 24).

13. Hariguchi teaches the invention (claim 41) as claimed including a method of initializing hardware comprising:

transferring network addresses to a CAM based on an index to a hash table (e.g., see Figures 2A-2B);

transferring port numbers to an output memory device responsive to the CAM (e.g., see Figures 2A-2B);

modifying bit prefix values to obtain a ternary representation (e.g., see col. 6, lines 25-28);

calculating bank run length information (e.g., see col. 3, lines 8-20); and,

loading starting address and bank run length information into a plurality of memory devices (e.g., see col. 4, line 31 to col. 5, line 63).

As to claim 42, Hariguchi teaches periodically transferring invalid network addresses to the CAM (e.g., see col. 4, line 31 to col. 5, line 63).

As to claim 44, Hariguchi teaches the bank run length information includes an end address and an address span (e.g., see col. 4, line 31 to col. 5, line 63).

35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 30, 35 and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hariguchi et al. in view of Khanna et al.

16. Hariguchi teaches the elements of the independent claims as given above. Hariguchi does not specifically teach the CAM being comprised of SRAM, however, Hariguchi does teach using a CIDR Processor as the given CAM. Khanna teaches CIDR address routing which can be implemented using SRAM cells (e.g., see col. 9, 1-17). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Khanna with the teachings of Hariguchi because both references teach using a CIDR or Classless Inter Domain Routing scheme and the CIDR scheme can be implemented using SRAM type memory.

Conclusion

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reba I. Elmore, whose telephone number is (703) 305-9706. The examiner can normally be reached on M-TH from 7:30am to 6:00pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the art unit supervisor for AU 2187, Donald Sparks, can be reached for general questions concerning this application at (703) 308-1756. Additionally, the official fax phone number for the art unit is (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Tech Center receptionist whose telephone number is (703) 305-3800/4700.

Reba I. Elmore
Primary Patent Examiner
Art Unit 2187

September 20, 2004